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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 2068.0030000

U.S. APPLICATION NO. (IF KNOWN, SEE 37 C.F.R. § 1.5): To be assigned 10/089517

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/NZ00/00189	September 29, 2000	September 29, 1999

TITLE OF INVENTION: Improvements Relating to EER Transmitters

APPLICANT(S) FOR DO/EO/US: Stephen Ian Mann

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
   a. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
3. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
4. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
5. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
6. ☒ Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
7. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 372(c)(3)).
8. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
9. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern other document(s) or information included:

10. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
11. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
12. A FIRST preliminary amendment.
13. ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
17. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
18. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
19. ☒ Other items or information:
    a. International Preliminary Examination Report with Annexes;
    b. Application Data Sheet;
    c. Authorization to Treat a Reply as Incorporating an Extension of Time under 37 C.F.R. § 1.136(a)(3);
    d. Two return postcards.

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
To be assigned 10/089517	PCT/NZ00/00189	2068.0030000

21. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) ..... **$ 100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

Claims	Number Filed	Number Extra	Rate		
Total Claims	8 - 20 =	0	X **$18.00**	$	
Independent Claims	1 - 3 =	0	X **$84.00**	$	
Multiple dependent claim(s) (if applicable)			+ **$280.00**	$	
TOTAL OF ABOVE CALCULATIONS =				$ 1020.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$	
SUBTOTAL =				$ 1020.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 1020.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
TOTAL FEES ENCLOSED =				$ 1020.00	
				Amount to be refunded:	$
				charged:	$

a. ☒ A check in the amount of $ 1020.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-0036. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Previde credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit Under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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DT17 Rec'd PCT/PTO 23 JUL 2002

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July 23, 2002

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Commissioner for Patents
Washington, D.C. 20231

Re: U.S. Utility Patent Application
U.S. Appl. No. 10/089,517 (unofficial) (which is the U.S. National Stage of PCT Appl. No. PCT/NZ00/00189, I.A. Filed: September 29, 2000)
For: **Improvements Relating to EER Transmitters**
Inventor: Stephen Ian Mann
Our Ref: 2068.0030000

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Preliminary Amendment; and
2. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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APPLICATION INFORMATION

Title Line One:: Improvements Relating to EER Transmitter
Title Line Two:: s
Total Drawing Sheets:: 9
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: 2068.0030000
Secrecy Order in Parent Appl.?:: No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 28393

CONTINUITY INFORMATION

This application is a:: 371 OF
> Application One:: PCT/NZ00/00189
Filing Date:: 09-29-2000

PRIOR FOREIGN APPLICATIONS

Foreign Application One:: 338097
Filing Date:: 09-29-1999
Country:: New Zeland
Priority Claimed:: Yes

Source:: PrintEFS Version 1.0.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Stephen Ian Mann

Appl. No.: 10/089,517 (unofficial)
U.S. National Stage of: PCT/NZ00/00189

I.A. Filed: September 29, 2000

For: **Improvements Relating to EER Transmitters**

Art Unit: To be assigned

Examiner: To be assigned

Atty. Docket: 2068.0030000

Preliminary Amendment

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-captioned application, Applicants submit the following Amendment and Remarks. This Amendment is provided in the following format:

(A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;

(B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.111 and MPEP 714; and

(C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments

In the Claims:

Please add the following new claims 9-14:

9. (New) An amplification system for a radio transmitter comprising:

a digital processing subsystem which determines envelope information and phase information from a baseband input signal;

a phase modulator which generates a substantially constant amplitude radio frequency (RF) signal having phase determined by the phase information;

an envelope modulator which generates an amplitude modulation signal determined by the envelope information;

an amplifier which generates an RF output signal from the constant amplitude signal and the amplitude modulation signal; and

a Cartesian feedback path from the output of the amplifier to the digital processing subsystem.

10. (New) A system according to claim 9, wherein:

the digital processing subsystem varies at least one of the phase information and the envelope information according to the Cartesian feedback.

11. (New) A system according to claim 9, wherein:

the digital processing subsystem predistorts at least one of phase modulation and envelope modulation of the output signal according to the Cartesian feedback.

12. (New) An amplification system for a radio transmitter comprising:

a digital processing subsystem which determines envelope information and phase information from a baseband input signal;

a phase modulator which generates a substantially constant amplitude radio frequency (RF) signal having phase determined by the phase information;

an envelope modulator which generates an amplitude modulation signal determined by the envelope information;

an amplifier which generates an RF output signal from the constant amplitude signal and the amplitude modulation signal; and

a predistorter in the digital processing system that distorts at least one of the phase information and the envelope information according to feedback from the output of the amplifier.

13. (New) A system according to claim 12, wherein:

the predistorter is coupled to the phase modulator and/or the envelope modulator.

14. (New) A system according to claim 12, wherein:

the feedback includes inphase and quadrature components derived from the output of the amplifier.

Remarks

Entry of the foregoing Preliminary Amendment into the above-identified application, prior to examination thereof, is respectfully requested.

Upon entry of the foregoing Amendment, claims 1-14 are pending, with claims 1, 9 and 14 being the independent claims. Claims 9-14 are sought to be added. These changes are believed to introduce no new matter.

The Examiner is invited to telephone the undersigned representative if an interview is believed to be useful for any reason.

Respectfully submitted,

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SKGF_DC1:28527.1

Version with markings to show changes made

Claims 9-14 have been added.

IMPROVEMENTS RELATING TO EER TRANSMITTERS

FIELD OF THE INVENTION

This invention relates to amplification systems for radio frequency signals and in particular but not solely to envelope elimination and restoration (EER) techniques for radio transmitters. More specifically the invention relates to feedback, and phase or envelope modulation aspects of these techniques. In one embodiment a phase lock loop (PLL) arrangement enables phase modulation and adjustment.

BACKGROUND TO THE INVENTION

Mobile communication systems require high frequency power amplifiers for both base station transmitters and portable units carried by users. These amplifiers operate most efficiently at saturation in the non-linear range of their input/output characteristics. Efficiency is important for battery life and weight in the portable units while linearity is important for base stations with multiple carrier transmission. A number of techniques have been developed to compensate for non-linear amplifier operation. Techniques involving modulation feedback from the amplified signal can be divided in two groups depending on how the modulating signal is represented in the baseband. Cartesian amplification systems apply a feedback signal to quadrature components of the modulating signal. Polar loop amplification systems are based on EER techniques with addition of envelope and phase feedback arrangements. The phase feedback forms a PLL although envelope feedback alone may be used.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide for improved amplification systems based on EER techniques. In general terms the invention may use Cartesian feedback and/or predistortion feedback in these techniques for linearisation. In one embodiment the invention implements a PLL with phase modulation by way of a fractional-N divider.

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Received 06 July 2001
PCT/NZ00/00189

Accordingly the invention may broadly be said to consist in an amplification system for a radio transmitter comprising: a processing subsystem which determines envelope information and phase information from a baseband input signal, a phase modulator which generates a substantially constant amplitude signal having phase determined by the phase information, an envelope modulator which generates an amplitude modulation signal determined by the envelope information, and an amplifier which generates an output signal from the constant amplitude signal and the amplitude modulation signal.

The phase modulator may include a PLL or other such as a quadrature modulator. The PLL preferably includes a frequency divider which is modulated according to the phase information. Preferably the envelope modulator includes a pulse width modulator or a sigma delta modulator.

The processing subsystem may modify the envelope or phase information according to various forms of Cartesian feedback from the output signal from the amplifier. The processing subsystem may also or alternatively provide a predistort signal to the phase modulator or the envelope modulator in a variety of ways.

BRIEF LIST OF FIGURES

Preferred embodiments of the invention will be described with reference to the drawings of which:

Figure 1 schematically shows a radio transmitter with amplification of a signal by a polar loop feedback system,

Figure 2 shows an amplification system in a general form according to the invention,

Figure 3 shows one embodiment of the system with Cartesian feedback,

Figure 4 shows another embodiment of the system with feedback for predistortion,

Figure 5 shows an alternative embodiment of the system with feedback for predistortion,

Figure 6 shows another embodiment with phase modulation by way of a phase lock loop,

Figure 7 shows a PLL arrangement for use in the system of Figure 6,

Figure 8 shows an alternative embodiment using a phase lock loop,

Figure 9 shows a PLL arrangement for use in the system of Figure 8,

Figure 10 shows a digital envelope feedback arrangement,

Figure 11 shows an analog envelope feedback arrangement.

Figures 12, 13, 14 show amplitude modulators in more detail, and

Figure 15 shows a phase modulation arrangement.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to the drawings it will appreciated that the invention may be implemented in various forms and that these embodiments are described by way of example only. Details of existing mobile communication systems will also be known to a skilled reader and need not be given here.

Figure 1 shows EER implemented in a traditional polar loop system. An incoming RF signal I is converted by analog block 10 into polar signals Θ, r respectively containing phase and envelope information. A phase controlled loop including power amplifier 11 operating in saturation then generates an output signal S according to the information, for transmission by antenna 12. The phase controlled loop forms a PLL which receives signal Θ and provides a constant amplitude signal to the non-linear amplifier. A power supply to the amplifier receives signal r and thereby controls gain of the amplifier to restore envelope information and produce signal S. The PLL includes a phase comparator or detector 13 which compares the phases of signal Θ and feedback from signal S to determine the frequency of a voltage controlled oscillator 14. The oscillator in turn provides the constant amplitude signal to the amplifier. Signal r is also modified by addition in block 15 of feedback from signal S. The feedback arrangement includes an optional frequency downconverter 16 followed alternatively for signals Θ, r by an amplitude limiter 17 and envelope detector 18.

Figure 2 gives a schematic overview of the invention in a very general form. A digital sub-system or processor arrangement 20, such as a DSP, determines phase and envelope signals P and E from an incoming signal B. A power amplifier 21 generates an output signal S which contains B modulated on a radio frequency carrier. A phase modulator 22 such as a PLL or quadrature modulator forms a phase modulation path which feeds the amplifier, although in some cases the amplifier may be part of the modulator. An envelope modulation path varies the amplifier gain by way of a modulator 23, which may vary a power supply to one stage of the amplifier for example. The phase and envelope signals P and E may include several components such as predistortion signals as indicated below. A feedback path from the output of the amplifier to the digital sub-system may take many forms, preferably a Cartesian loop which combines with quadrature signals in the digital sub-system. Feedback arrangement 24 may include a range of process components such as an analog detector at the output of the amplifier, an analog-to-digital converter (ADC) for single or quadrature signals from the detector, and other specialised components such as an optimiser for predistortion.

Figure 3 shows one embodiment with several components of the digital sub-system in Figure 2. Baseband signal B is converted to quadrature signals I, Q which are input to a phase extraction process 30 which in turn provides a phase signal for the modulator 22, and input to an envelope detector 31 which provides an envelope signal for the modulator 23. Feedback from the amplifier 21 is processed by a detector 34, ADC 35 and further digital processing stage 36 as may be required before addition to the quadrature signals I, Q at combiners 37, 38. The feedback arrangement therefore forms a Cartesian loop which tends to suppress imperfections in modulation of the amplifier and generally to linearise the amplification process. The loop may be partly or fully analog. Baseband sampling, or low or high intermediate frequency sub-sampling may be used in a partly digital Cartesian loop.

Figures 4 and 5 are other embodiments of Figure 2 involving adaptive predistortion of the quadrature signals I, Q. They also incorporate a feedback arrangement which may or may not be a Cartesian loop such as shown in Figure 3. One advantage of predistortion without a Cartesian loop is the increased stability provided by an open rather than closed loop system. In Figure 4 a digital predistorter 40 determines a

distortion of the quadrature signals before input to the phase extraction and envelope detection stages. In Figure 5 a predistorter 50 determines separate distortion signals for the phase and envelope modulators. An optimisation process depending on the open loop feedback is normally required in each case.

Figure 6 shows another embodiment of an amplification system based on EER according to the invention. Phase and envelope signals P and E are again formed from an input B. A PLL frequency synthesiser 60 containing a frequency divider such as shown in Figure 7 forms a phase modulation path which feeds the amplifier. An envelope modulation path varies the amplifier gain by way of a modulator 61. The digital sub-system also preferably determines a phase offset signal O provided to the PLL over an offset adjustment path as described further below. This provides a fine adjustment of the phase of signal S if required to compensate distortion, and also equalises discrepancies between the phase and envelope modulation paths. A feedback arrangement including detection of envelope and/or phase distortion in signal S preferably provides a feedback signal F for the digital sub-system. A detector and ADC system 24 may be implemented in various ways either separately or incorporated partly in the sub-system. An alternative embodiment in which the amplifier forms part of the PLL is described in Figure 8.

Figure 7 shows a PLL arrangement having a frequency divider which could be used in the embodiment of Figure 6. The arrangement produces an output signal having a frequency which is an integer or fractional multiple of a reference signal and which is modulated according to the phase signal P. A voltage controlled oscillator 70 receives a control signal from phase comparator 71 by way of loop filter 72, and produces a constant amplitude output for the amplifier 21. The loop filter generally integrates an output provided by the comparator according to phase differences between a reference signal from frequency reference 73 and a feedback signal from the controlled oscillator. A phase offset may be introduced between the reference and feedback signals by signal O from the digital sub-system 20, according to feedback from amplifier 21. This may control the action of an additional current source or sink at the input to the loop filter, for example. A frequency divider 74 under control of a modulator 75 introduces phase signal P from the digital sub-system. The modulator is preferably a sigma-delta arrangement which determines

an instantaneous integer value N for the divider in accord with a clock signal from the output of the divider. Signal P forms a digital control word for the modulator.

Figure 8 shows another embodiment of an amplification system based on EER according to the invention. The arrangement is generally similar to that of Figure 6 except that some or all of the stages represented by amplifier 21 and fed by PLL 60 are now included within PLL 90, such as shown in Figure 9. This has an advantage that AM-PM phase errors caused by the amplifier stages are inherently corrected, so that there may be less requirement for a phase adjustment by offset signal O to compensate distortion. The signal may still be required to equalise discrepancies between the phase and envelope modulation paths. Coarse adjustment by a full cycle of the digital sampling period might still be required. On the other hand delay around the loop may be increased with loss of stability and possibly smaller bandwidth. Inclusion of amplification stages introduces additional delay in the loop. The gain and therefore bandwidth must be reduced to maintain stability.

Figure 9 shows a PLL arrangement having a frequency divider which could be used in the embodiment of Figure 8. The arrangement is generally similar to that of Figure 7 except that power amplifier stages 91 being some or all stages of the amplifier 21 in Figure 7, are included in the loop. Envelope information from the digital sub-system 22 is used to modulate the gain of the amplifier stages by way of signal E as before. A limiter 72 is also included to remove the envelope information from signal S before input to the divider 74. The limiter may form part of the input circuitry of the dividers, such as a high gain differential input of the kind found in pre-scalers commonly used in frequency synthesisers.

Figures 10 and 11 show digital and analog systems for obtaining envelope feedback from the power amplifiers 21 or 71 to determine a signal F for the digital sub-system 20. Digital feedback generally requires an envelope detector 100 which may be implemented in many ways. ADC 101 and DAC 102 are also generally required. Typically the amplitude modulator is a switching type to which the digital signal is directly applied. A combination function 105 of the feedback information with envelope information from the incoming signal B may then be used to form signal E for modulation of the amplifier. Analog feedback also requires an envelope

detector 110. A combination function 115 of the feedback with the envelope information takes place outside the digital sub-system before formation of signal E. Further feedback of distortion information may of course be provided by one or more signals F as shown in Figure 2, in addition to or instead of phase or envelope feedback. This would enable pre-distortion of the envelope and phase information signals E and P as described in relation to Figures 4 and 5. Processing to determine channel power or bandwidth effects might be used in signal S, for example.

Figure 12 shows a possible arrangement for linearisation of the amplitude modulator in more detail. Various options are shown in this illustration only some of which may be needed in practice. The power amplifier 120 in this example may be controlled by the modulator 121 by way of supply voltage or DC gate bias, as shown, or both. One or more of the drivers 122 to the amplifier might also be modulated. An envelope detector 123 provides an analog voltage signal from the digital processing sub-system 20 in Figure 2. The signal is mapped as required by a stage 124 to the modulator 121, or to the driver 122 through a digital-to-analog converter (DAC) 125. Localised feedback through ADC 126 can be used to assist linearisation of the modulator 121 if required.

Figures 13 and 14 show two alternatives for the amplitude modulator 23 of Figure 2 in more detail. An analog signal X is input to a pulse width modulator 130 in Figure 13 and a digital signal Y is interpolated to a sigma delta modulator in Figure 14. In both cases the modulator drives a switching transistor 131, 141 through a low pass filter 132, 142 to the amplifier 21. A single loop sigma delta modulator is generally most effective having a large dynamic range, and can be part of an all digital circuit.

Figure 15 show two alternative feedback paths which might be used to linearise the phase modulator 22 of Figure 2. The degree of linearity is generally required to match the AM-PM of the power amplifier 21. Either one or two drivers 151 of the amplifier may be encompassed in feedback. A limiter 150 is typically required in the latter case to remove amplitude modulation.

CLAIMS:

1. An amplification system for a radio transmitter comprising:

a processing subsystem which determines envelope information and phase information from a baseband input signal,

a phase modulator which generates a substantially constant amplitude signal having phase determined by the phase information,

an envelope modulator which generates an amplitude modulation signal determined by the envelope information, and

an amplifier which generates an output signal from the constant amplitude signal, and the amplitude modulation signal,

wherein the phase modulator includes a phase-lock-loop or a quadrature modulator, and the phase-lock-loop includes a frequency divider which is modulated according to the phase information.

2. A system according to claim 1 wherein:

the envelope modulator includes a pulse width modulator or a sigma delta modulator.

3. A system according to claim 1 wherein:

the frequency divider is modulated by a sigma-delta modulator which is controlled by the processing subsystem.

4. A system according to claim 1 wherein:

the processing subsystem modifies the envelope information according to Cartesian feedback from the output signal from the amplifier.

5 A system according to claim 1 wherein:

the processing subsystem modifies the phase information according to Cartesian feedback from the output signal from the amplifier.

6. A system according to claim 1 wherein:

the processing subsystem predistorts the phase modulation of the output signal according to the envelope information and feedback from the output signal.

7. A system according to claim 1 wherein:

the processing subsystem predistorts the phase modulation of the output signal by modifying the phase information.

8. A system according to claim 1 wherein:

the amplifier is part of the phase modulator.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 April 2001 (05.04.2001)

PCT

(10) International Publication Number
WO 01/24356 A1

(51) International Patent Classification[7]: H03C 5/00, H04L 27/34

(21) International Application Number: PCT/NZ00/00189

(22) International Filing Date:
29 September 2000 (29.09.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
338097 29 September 1999 (29.09.1999) NZ

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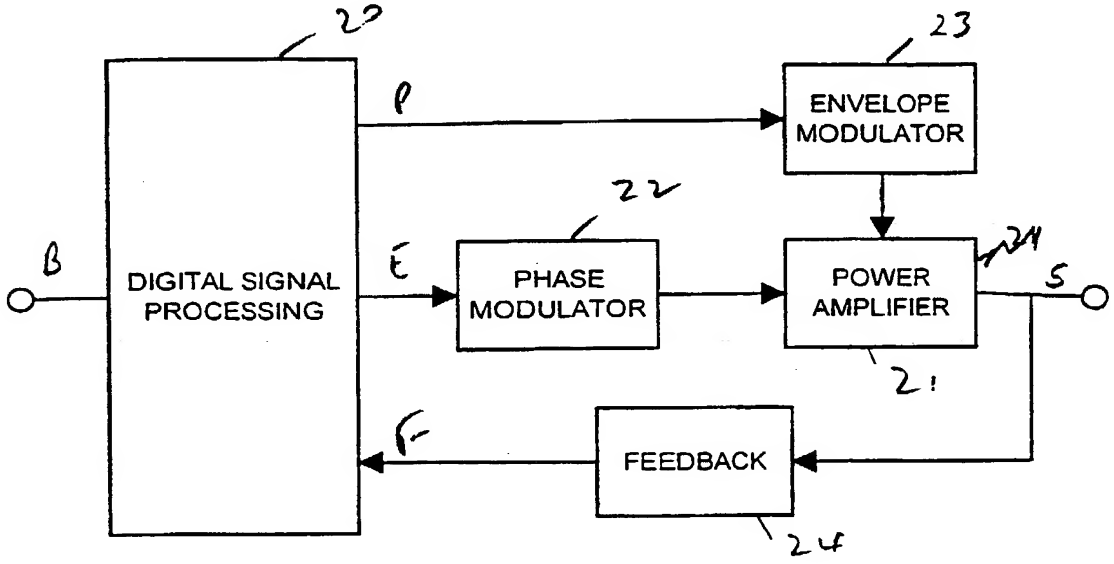
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: IMPROVEMENTS RELATING TO EER TRANSMITTERS



(57) Abstract: Amplification systems based on EER techniques, generally using digital methods to determine envelope and phase information. Cartesian or predistortion feedback is preferably used to improve a range of characteristics. Envelope modulation may be implemented in various ways such as a sigma delta modulator. Phase modulation may also be implemented in various ways such as a fractional N phase lock loop.

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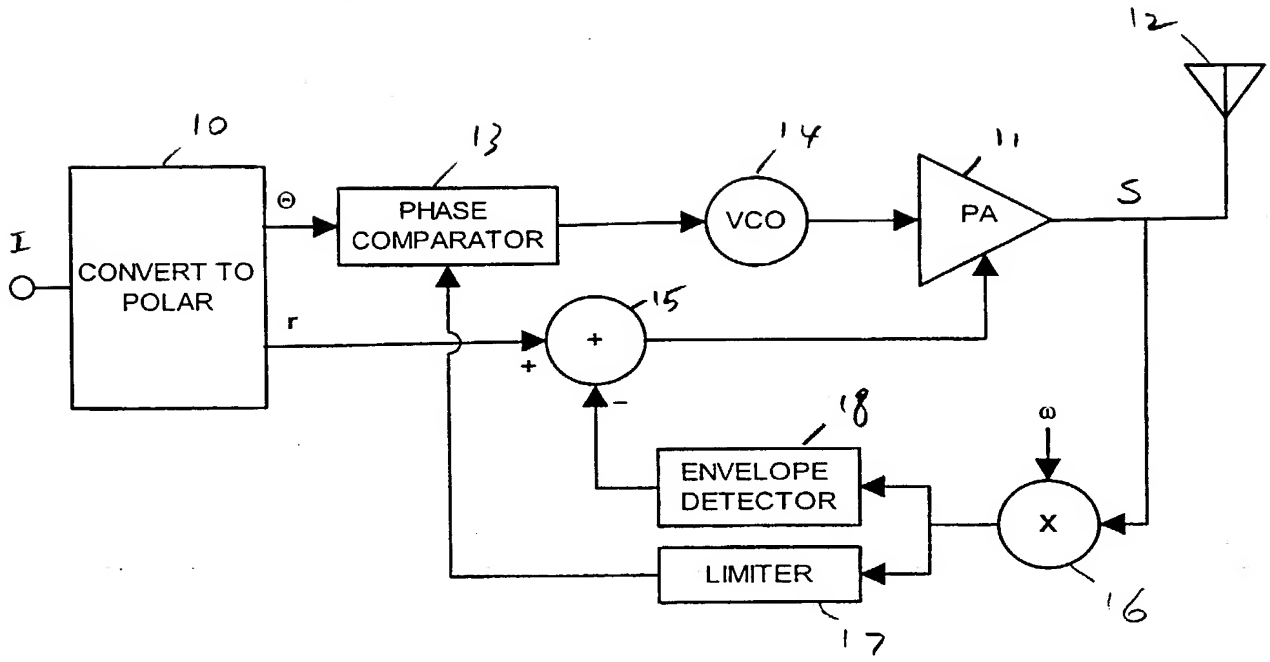
12
10
13
14
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I
CONVERT TO POLAR
Θ
PHASE COMPARATOR
VCO
PA
S
r
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+
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18
ω
ENVELOPE DETECTOR
X
LIMITER
16
17

FIGURE 1

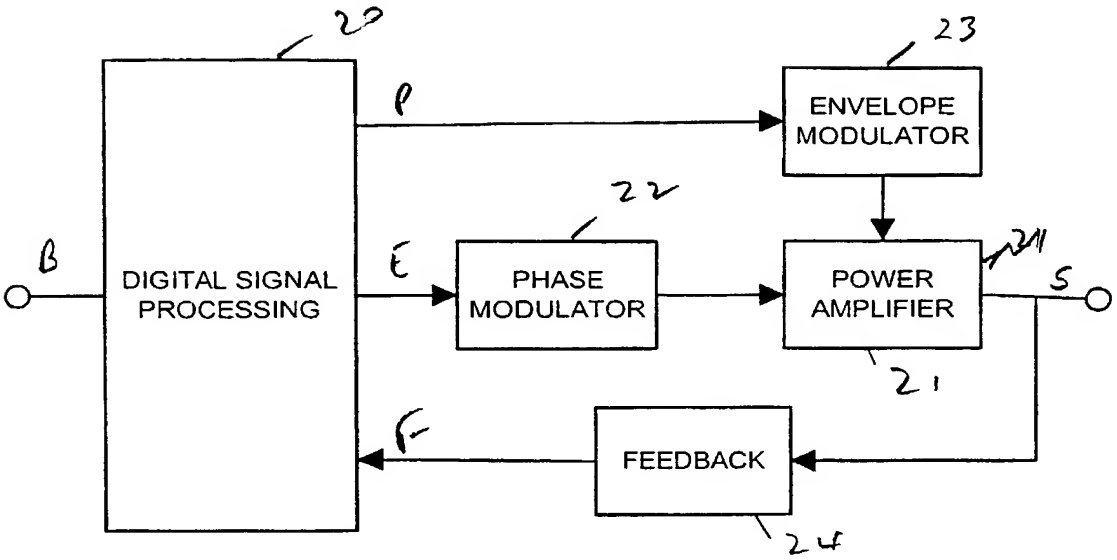

FIGURE 2

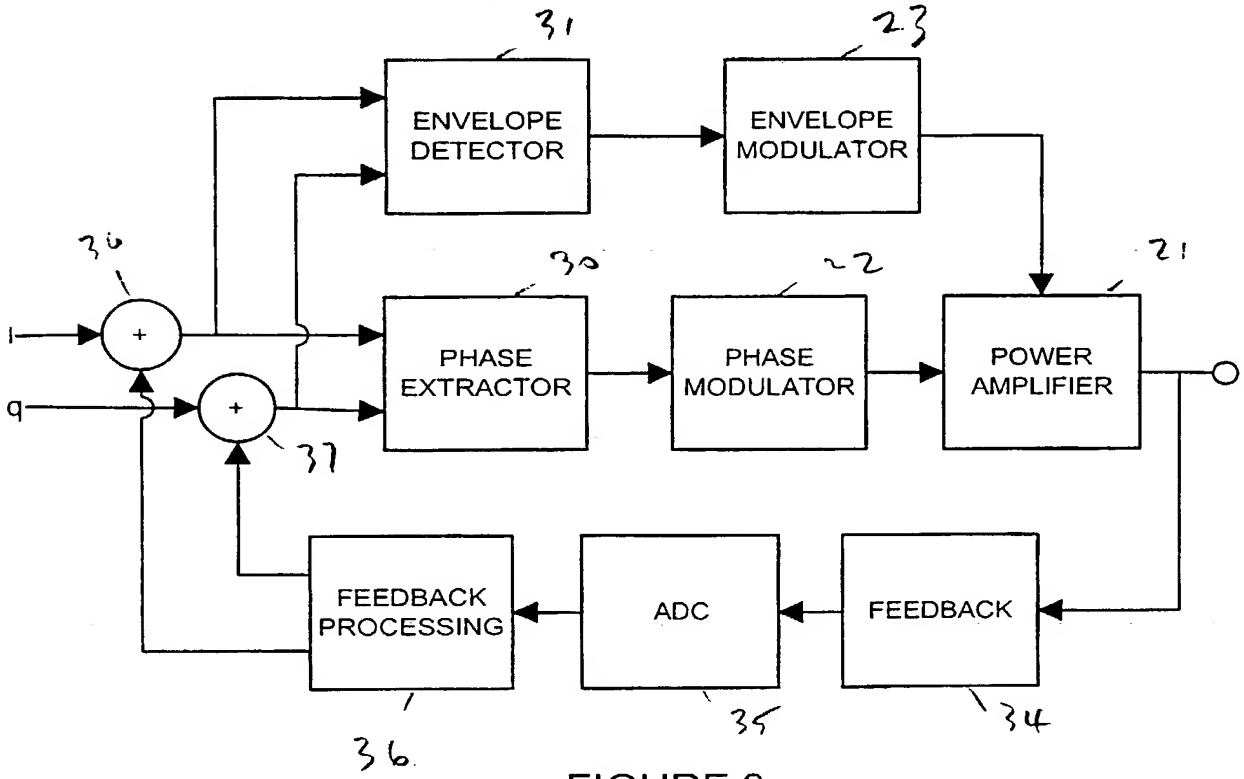

FIGURE 3

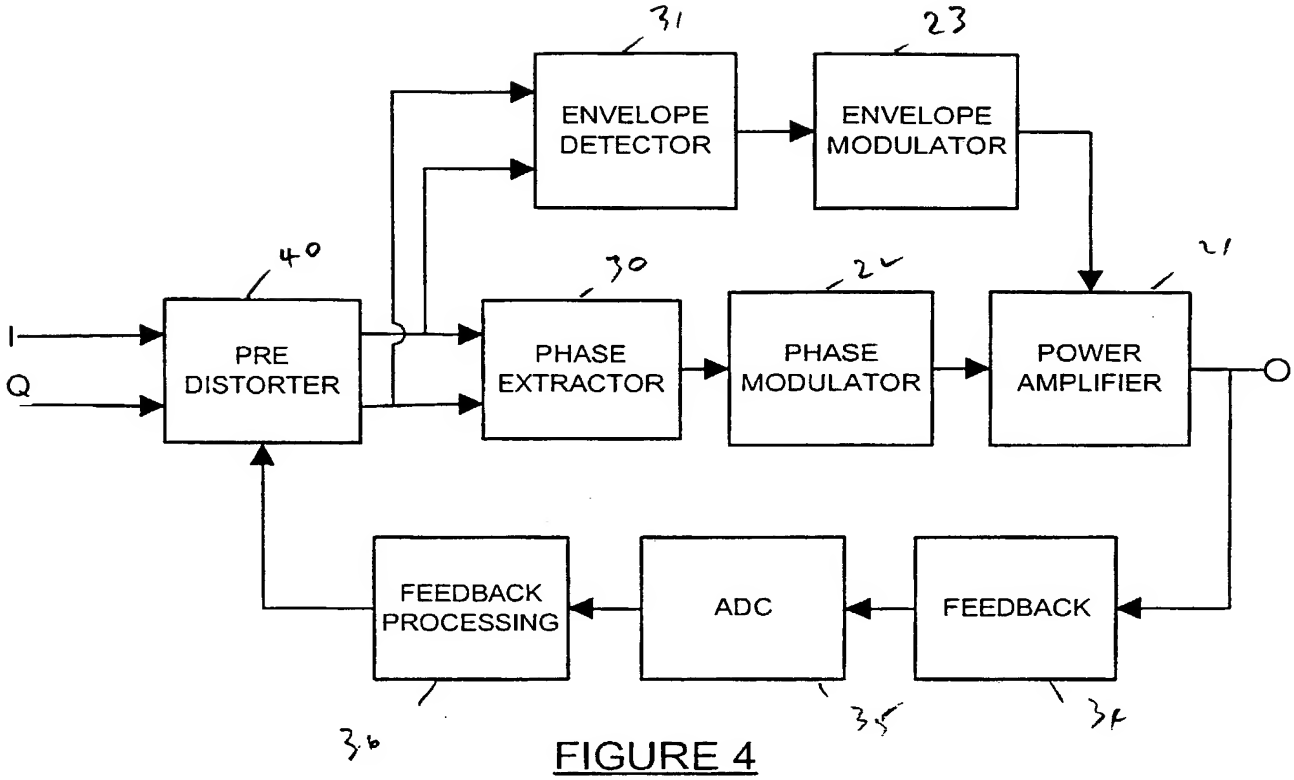

FIGURE 4

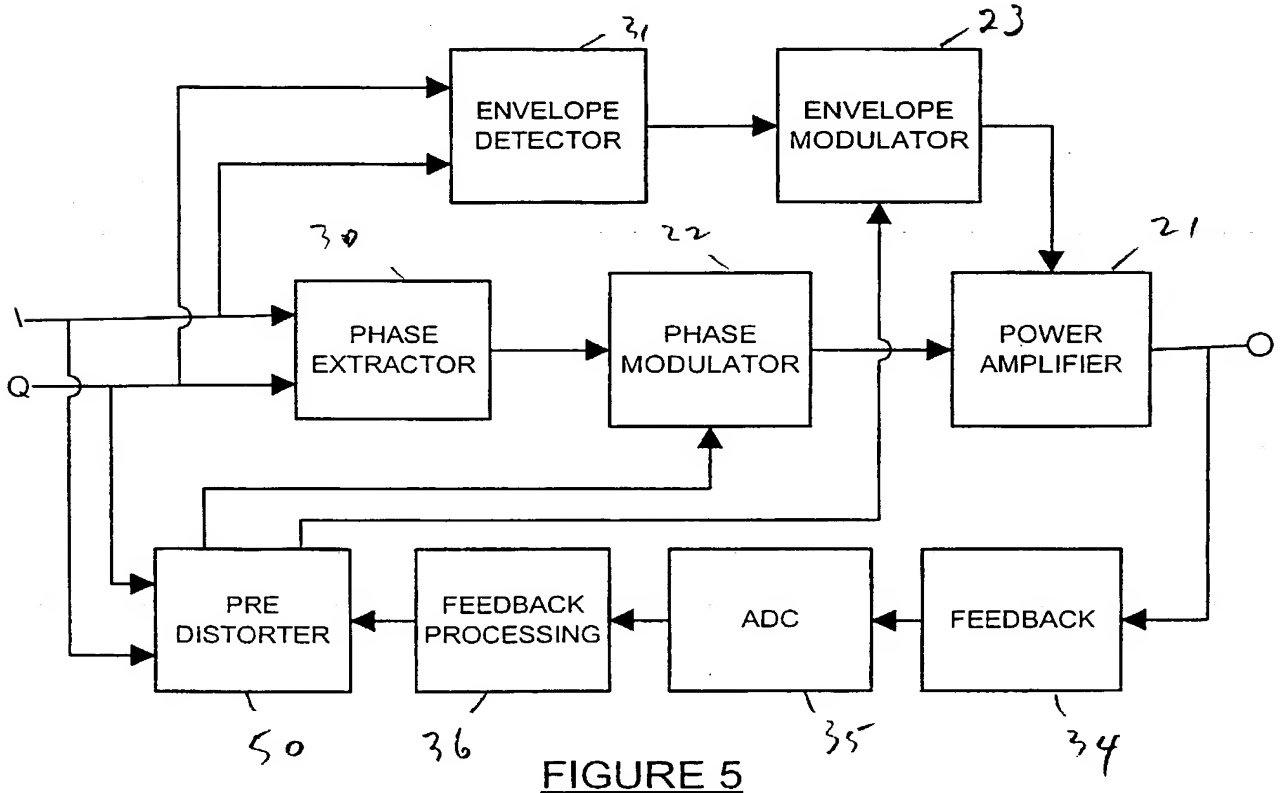

FIGURE 5

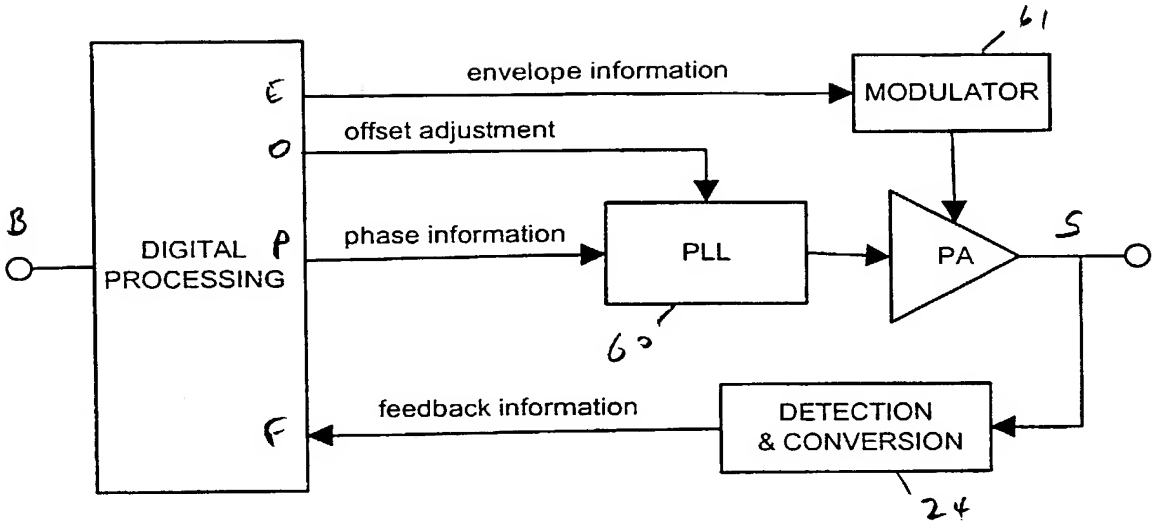

FIGURE 6

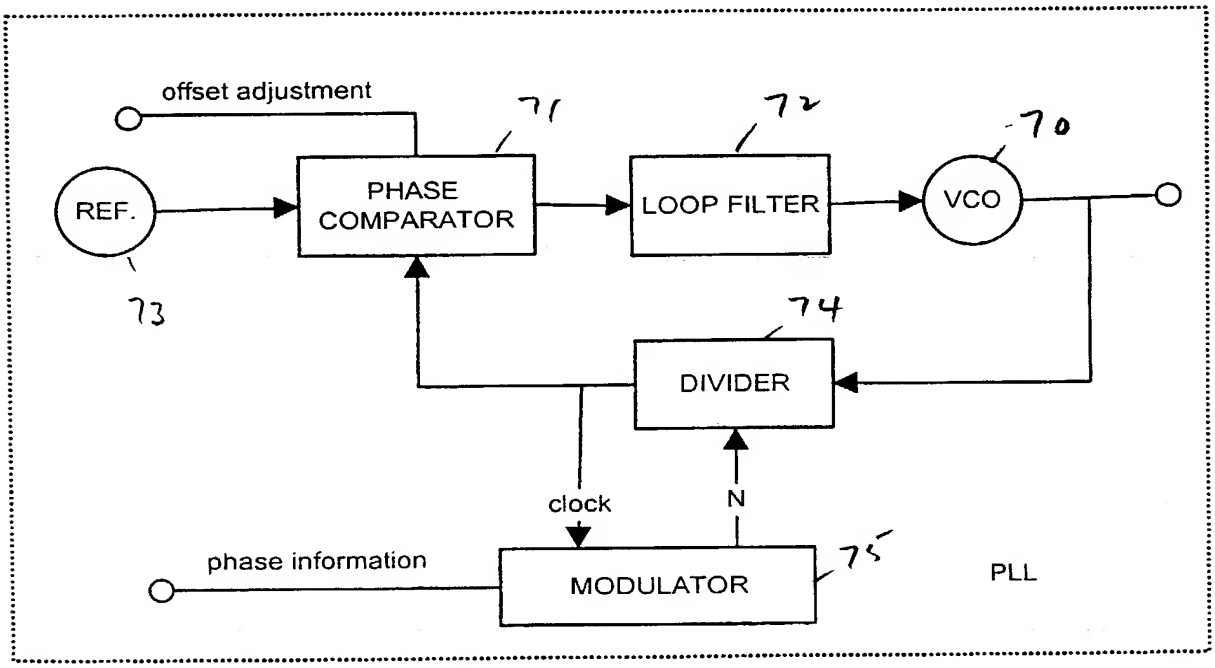

FIGURE 7

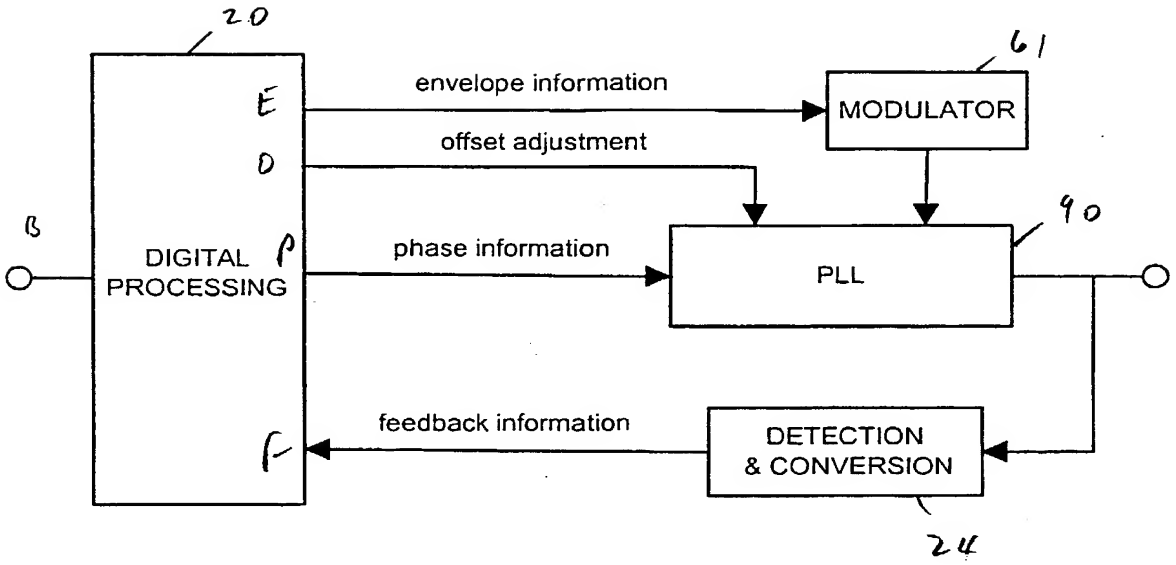

FIGURE 8

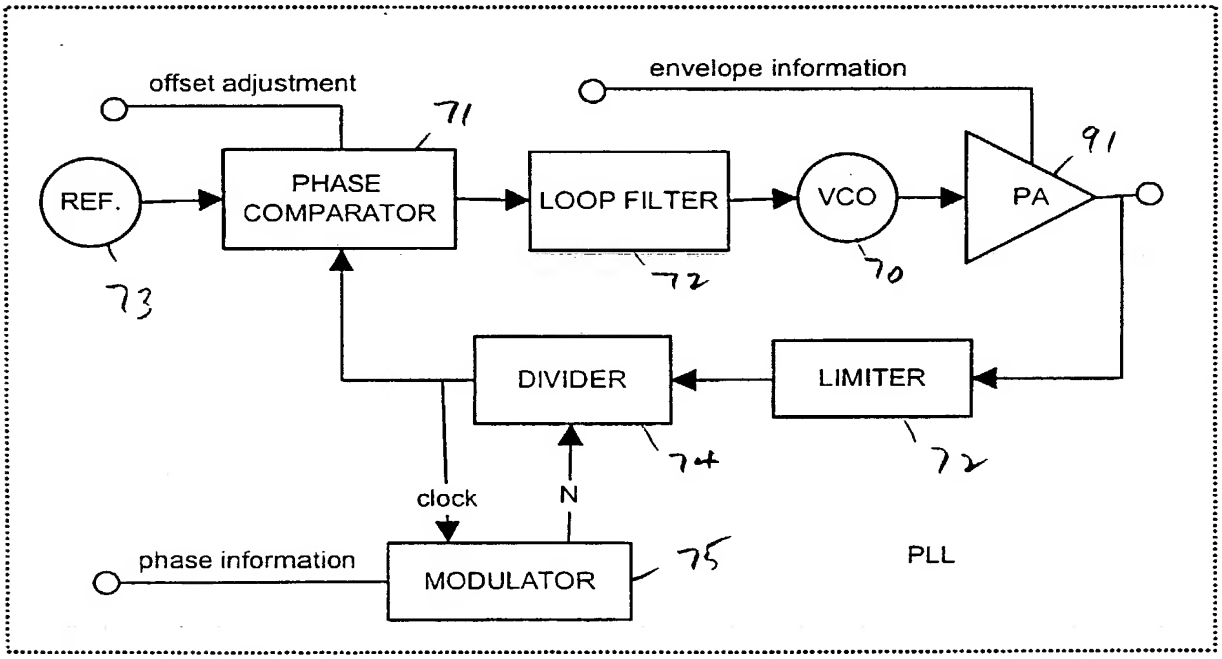

FIGURE 9

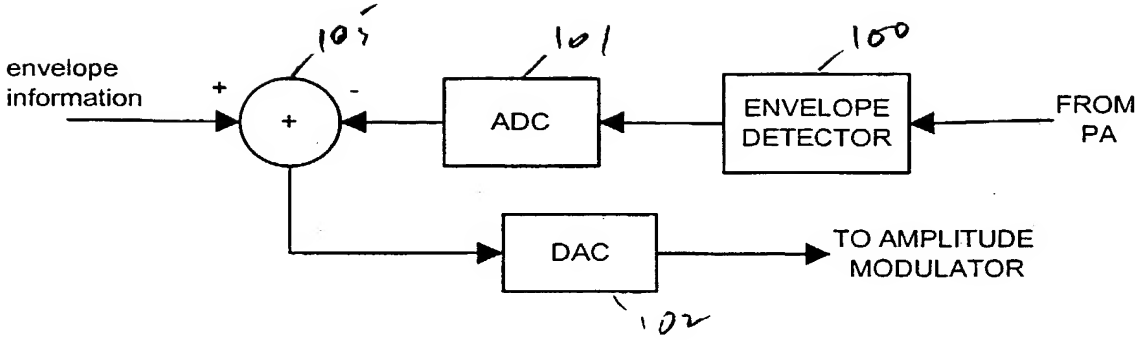

FIGURE 10

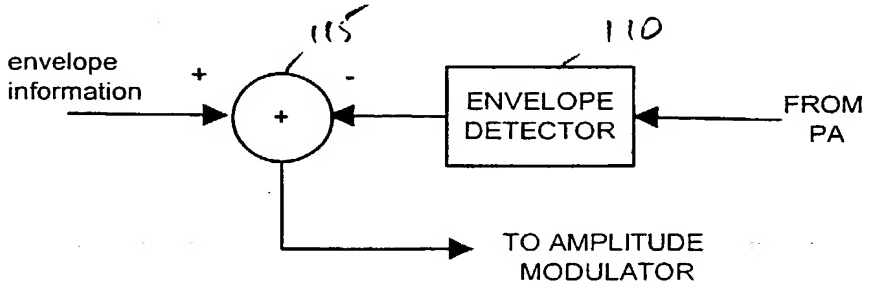

FIGURE 11

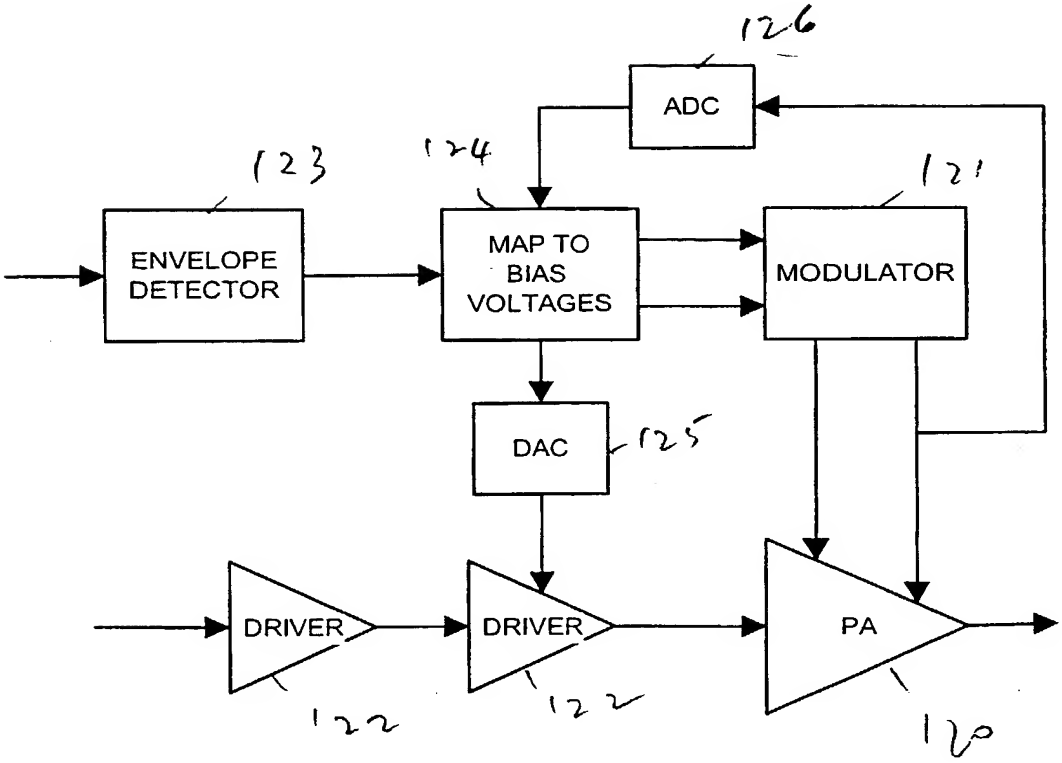
126
ADC
123
124
121
ENVELOPE DETECTOR
MAP TO BIAS VOLTAGES
MODULATOR
DAC
125
DRIVER
DRIVER
PA
122
122
120

FIGURE 12

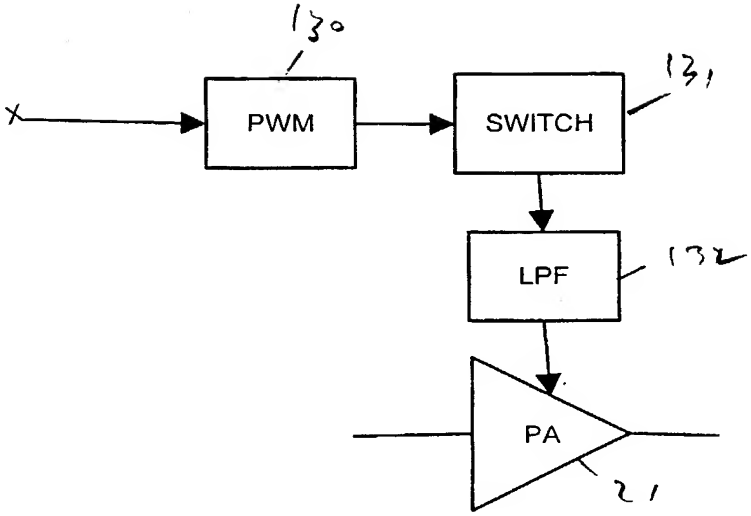

FIGURE 13

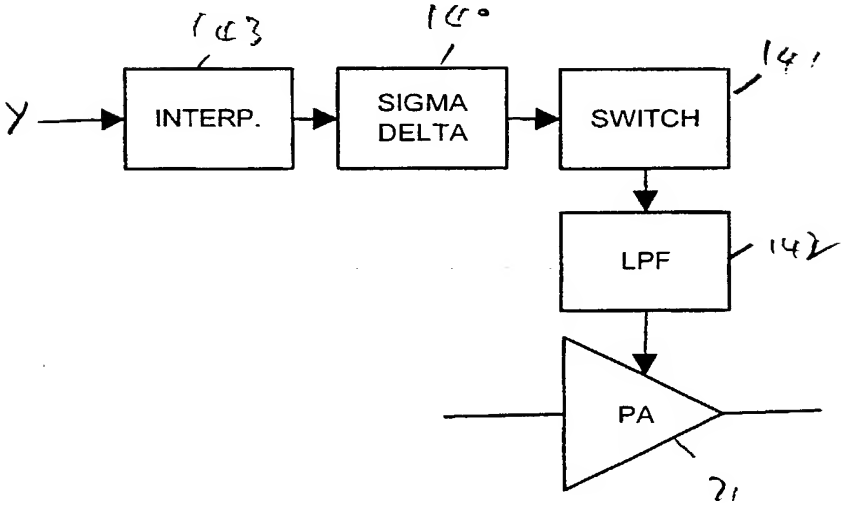

FIGURE 14

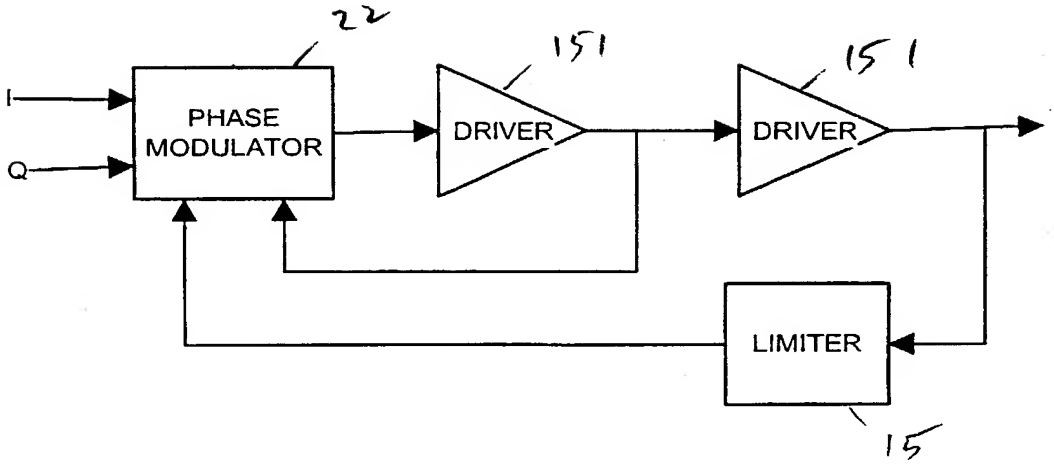

FIGURE 15

Declaration for Patent Application

Docket Number: 2068.0030000

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled: **Improvements Relating to EER Transmitters,**

the specification of which is attached hereto unless the following box is checked:

☒ was filed as United States Appl. No. 10/089,517 (which is the U.S. National Stage of PCT/NZ00/00189, international filing date: September 29, 2000).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information that became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f), or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
338097 (Application No.)	New Zealand (Country)	29/09/1999 (Day/Month/Year Filed)	☑ Yes ☐ No
PCT/NZ00/00189 (Application No.)	PCT (Country)	29/09/2000 (Day/Month/Year Filed)	☑ Yes ☐ No

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00

Full name of sole or first inventor	Stephen I. MANN
Signature of sole or first inventor	Date 18/3/03
Residence	Christchurch, New Zealand NZX
Citizenship	New Zealand
Mailing Address	c/o Tait Electronics Limited 558 Wairakei Road, Burnside
	Christchurch, New Zealand

(Supply similar information and signature for subsequent joint inventors, if any)